Remarks/Arguments

Claims 1 – 14 are pending in the application. Claims 1 and 13 are independent.

In the present amendment, claims 1 and 13 are amended. The support for the claim amendment may be found in Applicants' specification, for example, page 6, lines 6 – 10. No new matter is added.

Rejection of claims 1, 3 – 6, 10, 13 and 14 under 35 U.S.C. 102(b) as being anticipated by Novak et al. (US 6,496,906), hereinafter Novak

Applicants submit that for at least the following reasons, claims 1, 3 – 6, 10, 13 and 14 are patentable over Novak.

For example, independent claim 1, in part, recites:

> "*communication between the IC and the external RAM is performed via two or more channels, a channel is defined by its physical characteristics regarding at least throughput and latency.*" (Emphasis added)

Novak discloses a memory controller MCT 200 for a computer memory which decodes memory requests into individual primitive memory operations. The memory controller MCT 200 contains a SDRAM memory controller (SMC) 230, including an activate operation queue (AQ) 340, a pre-charge operation queue (PQ) 350, a read/write operation queue (RWQ) 360 and a read/write control queue (RWCQ) 365 (column 7, lines 43 – 48).

In the Office Action, page 2, the Office interprets these queues in Novak as corresponding to the channels in the present application. Applicants respectfully disagree.

Novak discloses that these queues (340, 350, 360) store commands received via the next request input 400. The commands that originate from the CPU 30 or the PCI bus 110 are treated as received via a single channel (treated as memory requesters 210) and are dedicated to a memory request arbiter MRA 220 (Fig. 1). The memory request arbiter MRA 220 contains a memory request decoder 310 (column 7, lines 50 – 53). All commands (activate, pre-charge,

read/write) are received via the next request input 400 (Fig. 2), thus all commands are received via one channel having the same characteristics regarding throughput and latency.

In contrast, the claimed invention requires that the communication between the IC and the external RAM is performed via two or more channels. Claim 1 is amended to clarify that a channel is defined by its physical characteristics regarding at least throughput and latency. As described above, Novak does only disclose one input channel described as memory requesters 210 for receiving commands from the CPU 30 (AMBA) and PCI bus 110 (input, output). Therefore, Novak fails to disclose the above claimed feature.

In addition, independent claim 1, in part, requires:

> "*further prioritizing the at least two commands having the same static priority on the basis of a dynamic priority allocation for the channels.*"

In Novak, only the commands issued by the activate operation queue (AQ) 340, the pre-charge operation queue (PQ) 350 and the read/write operation queue (RWQ) 360 are sent to an SDRAM priority multiplexer (SPM) 370. The SDRAM priority multiplexer (SPM) 370 implements the priority of the received commands according to their respective queues (340, 350, 360). A static priority is used for each queue, corresponding to a static priority for commands. The PQ 350 entries marked with hi have the highest priority, followed by the RWQ 360 entries, followed by the AQ 340 entries and finally followed by the standard PQ 350 entries (column 9, lines 1 – 5). This corresponds to a static priority of pre-charge operations marked as hi having the highest priority, followed by the read/write commands, followed by the activate commands and finally followed by the standard pre-charge commands. No further dynamic priority of these commands is disclosed by Novak.

In the Office Action, page 3, the Office alleged that Novak, column 7, lines 59 – 61, discloses a dynamic priority for each queue due to the fact that a first-in-first-out buffer is used. Applicants respectfully disagree.

Applicants respectfully submit that a first-in-first-out buffer does not provide a dynamic priority in general. Furthermore, it has to be noted that only commands of one buffer are prioritized according to the first-in-first-out principle by this buffer. Novak discloses that only commands of one type of are stored in one particular buffer. For example, the active commands are stored in an activate operation queue (AQ) 340, the pre-charge commands are stored in a pre-charge operation queue (PQ) 350 and the read-write commands are stored in a read/write operation queue (RWQ) 360. Only such a dynamic change would correspond to a dynamic priority allocation for channels.

However, as discussed above, in Novak, the commands that originate from the CPU 30 or the PCI bus 110 are treated as received via a single channel (treated as memory requesters 210) and are dedicated to a memory request arbiter MRA 220. The queues are prioritized in the SDRAM priority multiplexer SPM 370. This multiplexer uses solely a static priority scheme to prioritize entries (column 9, lines 1 – 5). Thus, Novak does not disclose any dynamic priority allocation for channels.

In view of at least the foregoing, Applicants submit that claim 1 is patentable over Novak. Independent claim 13 is different from and should be interpreted independently of claim 1. However, claim 13 contains many similar distinguishing features as in claim 1. Applicants essentially repeat the above arguments for claim 1 and apply them to claim 13, pointing out why claim 13 is patentable over Novak. Claims 3 – 6, 10 and 14 depend from and inherit all the features of claim 1. Thus claims 3 – 6, 10 and 14 are patentable for at least the reason that they depend from claim 1, with each claim containing further distinguishing features.

Withdrawal of the rejection of claims 1, 3 – 6, 10, 13 and 14 under 35 U.S.C. 102(b) is respectfully requested.

Rejection of claim 2 under 35 U.S.C. 103(a) as being unpatentable over Novak in view of Kirsch (GB 2,396,442)

Rejection of claims 7 and 9 under 35 U.S.C. 103(a) as being unpatentable over Novak in view of Wheeler et al. (US 6,983,350), hereinafter Wheeler

Rejection of claim 8 under 35 U.S.C. 103(a) as being unpatentable over Novak in view of Chen et al. (US 2003/0051108), hereinafter Chen

Rejection of claim 11 under 35 U.S.C. 103(a) as being unpatentable over Novak in view of LaBerge (US 2001/0044885)

Rejection of claim 12 under 35 U.S.C. 103(a) as being unpatentable over Novak in view of the power point entitled "Random Access Memory"

Applicants submit that none of the secondary references cited above can cure the deficiencies present in Novak as discussed above with respect to claim 1. Thus claims 2, 7 – 9, 11 and 12 are patentable for at least the reason that they depend from claim 1, with each claim containing further distinguishing features.

Withdrawal of the rejection of claims 2, 7 – 9, 11 and 12 under 35 U.S.C. 103(a) is respectfully requested.

Conclusion

Having fully addressed the Examiner's rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at (609) 734-6813, so that a mutually convenient date and time for a telephonic interview may be scheduled.

Respectfully submitted,
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